IN THE CLAIMS:

1. (Currently Amended) A method, comprising:

forming doped regions of a specified doping profile in a silicon region adjacent to a gate electrode having sidewall spacers formed thereon;

removing a native oxide layer from a surface layer of said doped regions;

after removing said native oxide layer, and without performing an oxidation process on said surface layer, removing ~~a surface~~ said surface layer of said doped regions by performing an etching process using a diluted etch solution; and

epitaxially growing a silicon layer on said doped regions after said surface layer is removed.

2. (Original) The method of claim 1, wherein said diluted etch solution comprises hydrogenated fluoride (HF), hydrogen peroxide (H_2O_2) and water.

3. (Original) The method of claim 1, wherein said diluted etch solution comprises ammonium hydroxide and hydrogen peroxide (APM).

4. (Canceled)

5. (Original) The method of claim 2, wherein said etch solution is applied by a spray tool.

6. (Original) The method of claim 2, further comprising rinsing said surface layer before or after applying said diluted etch solution.

7. (Original) The method of claim 2, wherein removing said surface layer includes intermittently applying said etch solution and cleaning said surface layer at least once during a discontinuation of etch solution application.

8. (Original) The method of claim 1, further comprising controlling a thickness of the removed surface layer by determining in advance an etch rate of said etch solution and adjusting an etch time.

9. (Currently Amended) The method of claim 1, wherein said surface layer comprises a plurality of contaminants and wherein the method further ~~comprising~~ comprises determining a penetration depth of ~~contaminations~~ said contaminants in said surface layer.

10. (Original) The method of claim 1, further comprising adjusting an under-etch of said sidewall spacers during removal of said surface layer.

11. (Currently Amended) The method of ~~claim 1~~ claim 10, further comprising forming a metal silicide in said grown silicon layer and said doped regions, wherein an effective lateral dimension is substantially determined by said under-etch.

12. (Canceled)

13. (Canceled)

14. (Currently Amended) A method, comprising:

forming doped regions of a specified doping profile in a silicon region adjacent to a gate electrode having sidewall spacers formed thereon;

removing a native oxide layer from a surface layer of said doped regions;

after removing said native oxide layer, and without performing an oxidation process on said surface layer, removing ~~a surface~~ said surface layer of said doped regions by using a diluted etch solution comprising hydrogenated fluoride (HF), hydrogen peroxide (H_2O_2) and water; and

epitaxially growing a silicon layer on said doped regions after said surface layer is removed.

15. (Canceled)

16. (Original) The method of claim 14, wherein said etch solution is applied by a spray tool.

17. (Original) The method of claim 14, further comprising rinsing said surface layer before or after applying said diluted etch solution.

18. (Original) The method of claim 14, wherein removing said surface layer includes intermittently applying said etch solution and cleaning said surface layer at least once during a discontinuation of etch solution application.

19. (Original) The method of claim 14, further comprising controlling a thickness of the removed surface layer by determining in advance an etch rate of said etch solution and adjusting an etch time.

20. (Currently Amended) The method of claim 14, wherein said surface layer comprises a plurality of contaminants and wherein the method further ~~comprising~~ comprises determining a penetration depth of ~~contaminations~~ said contaminants in said surface layer.

21. (Original) The method of claim 14, further comprising adjusting an under-etch of said sidewall spacers during removal of said surface layer.

22. (Currently Amended) The method of ~~claim 14~~ claim 21, further comprising forming a metal silicide in said grown silicon layer and said doped regions, wherein an effective lateral dimension is substantially determined by said under-etch.

23. (Currently Amended) A method, comprising:

forming doped regions of a specified doping profile in a silicon region adjacent to a gate electrode having sidewall spacers formed thereon;

removing a native oxide layer from a surface layer of said doped regions;

after removing said native oxide layer, and without performing an oxidation process on said surface layer, removing ~~a surface~~ said surface layer of said doped regions by using a diluted etch solution comprising ammonium hydroxide and hydrogen peroxide (APM); and

epitaxially growing a silicon layer on said doped regions after said surface layer is removed.

24. (Original) The method of claim 23, further comprising cleaning said surface layer prior to removing said surface layer so as to remove oxide residues.

25. (Original) The method of claim 23, further comprising rinsing said surface layer before or after applying said diluted etch solution.

26. (Original) The method of claim 23, further comprising controlling a thickness of the removed surface layer by determining in advance an etch rate of said etch solution and adjusting an etch time.

27. (Original) The method of claim 23, wherein said surface layer comprises a plurality of contaminants and wherein the method further ~~comprising~~ comprises determining a ~~typical~~ penetration depth of ~~contaminations~~ said contaminants in said surface layer.

28. (Original) The method of claim 23, further comprising adjusting an under-etch of said sidewall spacers during removal of said surface layer.

29. (Original) The method of claim 23, further comprising forming a metal silicide in said grown silicon layer and said doped regions, wherein an effective lateral dimension is substantially determined by said under-etch.

30.-37. (Canceled)